Abstract

A method and program product for verifying a logic design for proper operation of tri-state buses in the design, comprises, for each bus in the circuit design, determining the smallest cut set, a min-cut, of the logic controlling the bus, performing an exhaustive analysis on a min-cut set of logic, and performing a full exhaustive analysis of the bus when the exhaustive analysis on the min-cut set of logic is inconclusive. In a preferred embodiment, prior to performing the min-cut set analysis, implication based conflict-free and float-free analyses are performed on the bus.